AMENDMENT

In the Claims:

1. (Original) An integrated circuit manufactured by the method comprising the acts of:
(a.) providing a partially fabricated integrated circuit structure;
(b.) applying and curing spin-on glass, to form a first dielectric layer;
(c.) depositing dielectric material, to form a second dielectric layer over said first dielectric layer;
(d.) applying and curing spin-on glass, to form a third dielectric layer, to produce a stack including said third dielectric layer over said first and second dielectric layers;
(e.) performing a global etchback to substantially remove portions of said dielectric stack from high points of said partially fabricated structure, wherein at least a portion of said third dielectric layer remains after said global etchback;
(f.) deposition of an interlevel dielectric at least over said remaining third dielectric layer;
(g.) etching holes in said interlevel dielectric in predetermined locations; and
(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

2. (Original) The integrated circuit of claim 1, wherein said deposition step (c.) is plasma-enhanced.

3. (Original) The integrated circuit of claim 1, wherein said deposition step (c.) uses TEOS as a source gas.

4. (Original) The integrated circuit of claim 1, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and Am before said deposition step (b.).

5. (Original) The integrated circuit of claim 1, Hi wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000 .ANG. inclusive.

6. (Original) The integrated circuit of claim 1, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000 .ANG. inclusive.

7. (Original) The integrated circuit of claim 1, wherein said interlevel dielectric is a doped silicate glass.

8. (Original) An integrated circuit manufactured by the method comprising the acts of:
(a.) providing a partially fabricated integrated circuit structure;
(b.) applying and curing spin-on glass, to form a first dielectric layer;
(c.) depositing silicon dioxide, to form a second dielectric layer over said first dielectric layer;
(d.) applying and curing spin-on glass, to form a third dielectric layer to produce a dielectric stack including said third dielectric layer over said first and second layers;
(e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure, wherein at least a portion of said spin-on glass of said third dielectric layer remains after said global etchback;
(f.) deposition of an interlevel dielectric at least over said remaining spin-on glass of said third dielectric layer;
(g.) etching holes in said interlevel dielectric in predetermined locations; and
(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

9. (Original) The integrated circuit of claim 8, wherein said deposition step (c.) is plasma-enhanced.

10. (Original) The integrated circuit of claim 8, wherein said deposition step (c.) uses TEOS as a source gas.

11. (Original) The integrated circuit of claim 8, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

12. (Original) The integrated circuit of claim 8, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000 .ANG. inclusive.

13. (Original) The integrated circuit of claim 8, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000 .ANG. inclusive.

14. (Original) The integrated circuit of claim 8, wherein said interlevel dielectric is a doped silicate glass.

15. (Original) An integrated circuit manufactured by the method comprising the acts of:
(a.) providing a partially fabricated integrated circuit structure;
(b.) applying and curing spin-on glass, to form a first dielectric layer;
(c.) depositing dielectric material, to form a second dielectric layer over said first dielectric layer, said second dielectric layer having a thickness equal to or less than said first dielectric layer;
(d.) applying and curing spin-on glass, to form a third dielectric layer to produce a dielectric stack including said third dielectric layer over said first and second dielectric layers, said third dielectric layer having a thickness equal to or greater than said second layer;
(e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure, wherein at least a portion of said third dielectric layer remains after said global etchback;
(f.) deposition of an interlevel dielectric at least over said remaining second dielectric

layer;
(g.) etching holes in said interlevel dielectric in predetermined locations; and
(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

16. (Original) The integrated circuit of claim 15, wherein said deposition step (c.) is plasma-enhanced.

17. (Original) The integrated circuit of claim 15, wherein said deposition step (c.) uses TEOS as a source gas.

18. (Original) The integrated circuit of claim 15, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

19. (Original) The integrated circuit of claim 15, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000-5000 .ANG. inclusive.

20. (Original) The integrated circuit of claim 15, wherein said interlevel dielectric is a doped silicate glass.

21. (Original) The integrated circuit of claim 15, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000-5000 .ANG. inclusive.

22. (Original) An integrated circuit, comprising:
(a.) an active device structure, including therein a substrate, active device structures, isolation structures, and one or more patterned thin film conductor layers including an uppermost conductor layer; and
(b.) a planarization structure, overlying recessed portions of said active device structure, comprising a layer of sol-gel-deposited dielectric overlain by a layer of vacuum-deposited dielectric overlain by a further layer of sol-gel-deposited dielectric;

(c.) an interlevel dielectric overlying said planarization structure and said active device structure, and having via holes therein which extend to selected locations of said uppermost conductor layer; and

(d.) an additional thin-film patterned conductor layer which overlies said interlevel dielectric and extends through said via holes to said selected locations of said uppermost conductor layer.

23-38. (Cancelled)

39. (Previously Presented) A semiconductor structure, comprising:

a substrate;

a first layer of inorganic spin-on glass disposed on the substrate;

a first dielectric disposed on the first layer; and

a planarized second layer of inorganic spin-on glass disposed on the first dielectric.

40-42. (Cancelled)

43. (Previously Presented) The semiconductor structure of claim 39, further comprising:

a second dielectric disposed on the substrate; and

wherein the first layer of spin-on glass is disposed on the second dielectric.

44. (Previously Presented) The semiconductor structure of claim 39, further comprising:

a metal layer disposed on the substrate; and

wherein the first layer of spin-on glass is disposed on the metal layer.

45. (Previously Presented) The semiconductor structure of claim 39, further comprising:

a metal layer disposed on the substrate;

a second dielectric disposed on the metal layer; and

wherein the first layer of spin-on glass is disposed on the second dielectric.

46. (Previously Presented) The semiconductor structure of claim 39 wherein the first dielectric comprises a low-temperature oxide.

47. (Previously Presented) The semiconductor structure of claim 39, further comprising a planarized boundary that includes the planarized second layer of spin-on glass and a planarized portion of the first dielectric.

48. (Previously Presented) The semiconductor structure of claim 39, further comprising a planarized boundary that includes the planarized second layer of spin-on glass, a planarized portion of the first dielectric, and a planarized portion of the first layer of spin-on glass.